Virtual Capacitors for Single Phase Power Electronics Converters

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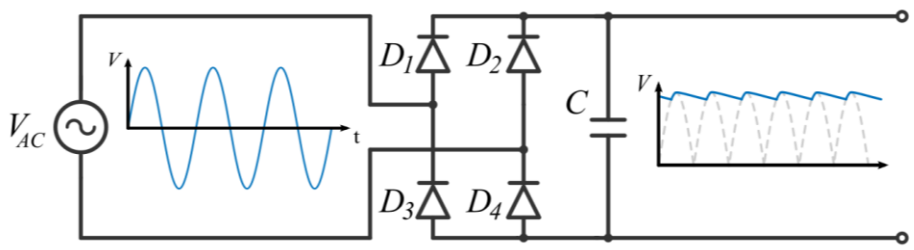
Outline

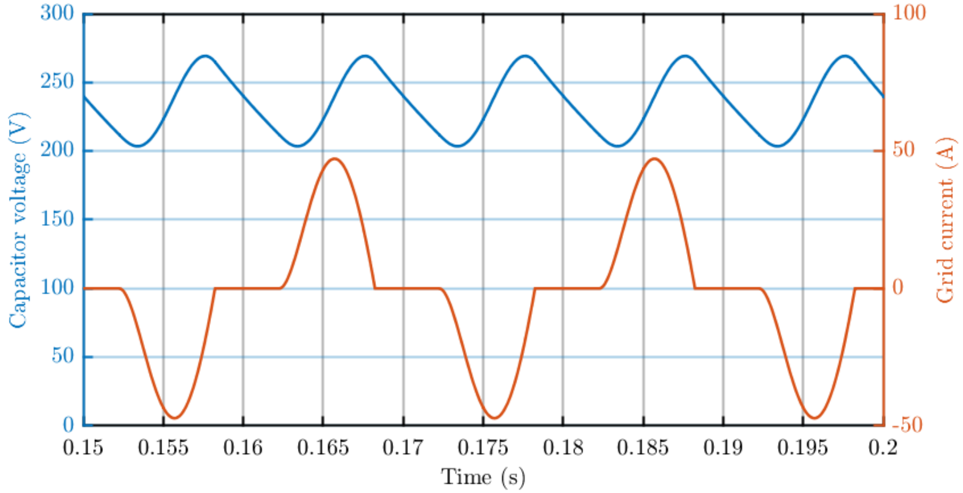
- Introduction and Motivation
- Active Front End
- Virtual Capacitor
- Experimental Validation
- Conclusions and personal contribution

Main issue: low power quality for single phase diode rectifiers

High harmonic content in the absorbed current → High THD

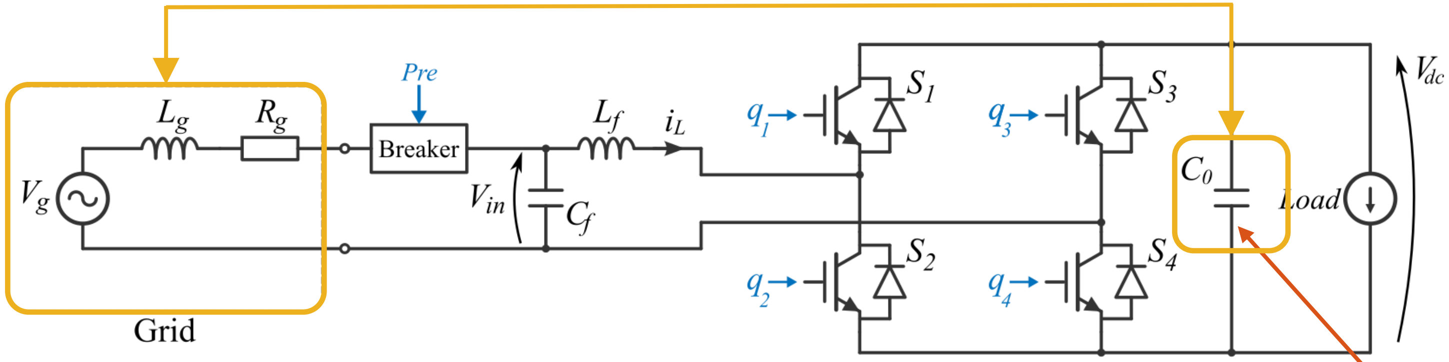
Pulsed Power
↓
Large capacitance is required to mitigate the ripple on the DC-bus → Low power density
↓
Most frequently used capacitors are electrolytic → Low reliability



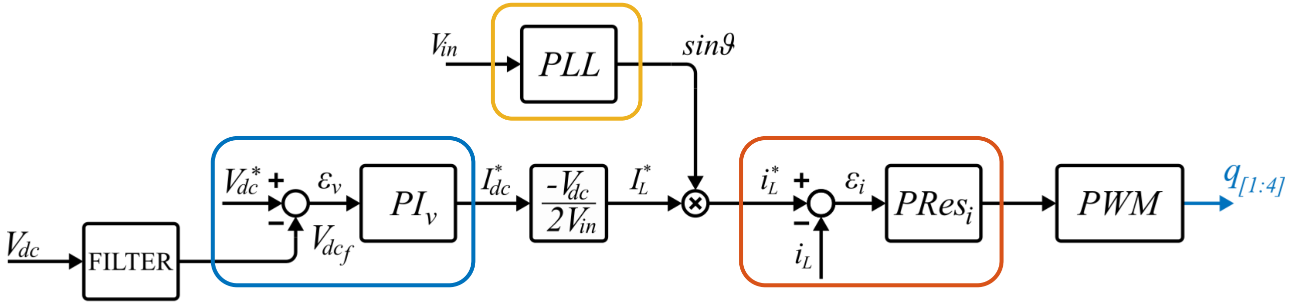


Active Rectifier With Boost Power Factor Correction (PFC) Stage

Pulsed energy exchanged at double the grid frequency

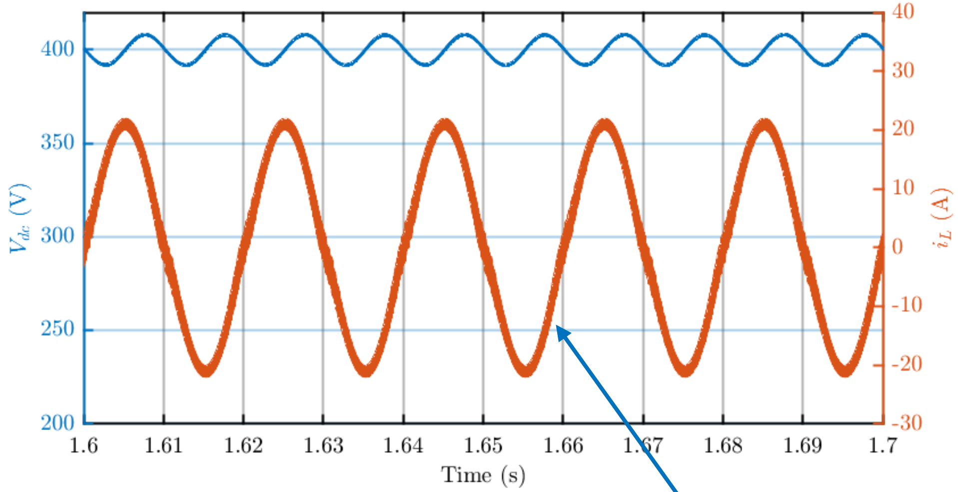


Grid synchronization



DC bus voltage loop

Grid current control

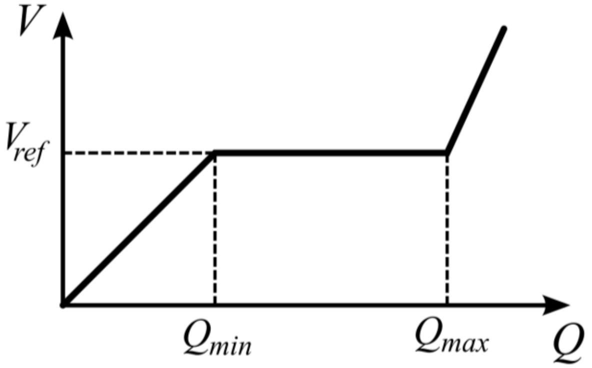


Still needs large capacitance to attenuate the ripple

Low THD

Virtual Capacitor

Based on the concept of nonlinear capacitor:



Instead of a linear dependence between Q and V it has a flat region in the range $[Q_{min}, Q_{max}]$

In the flat region

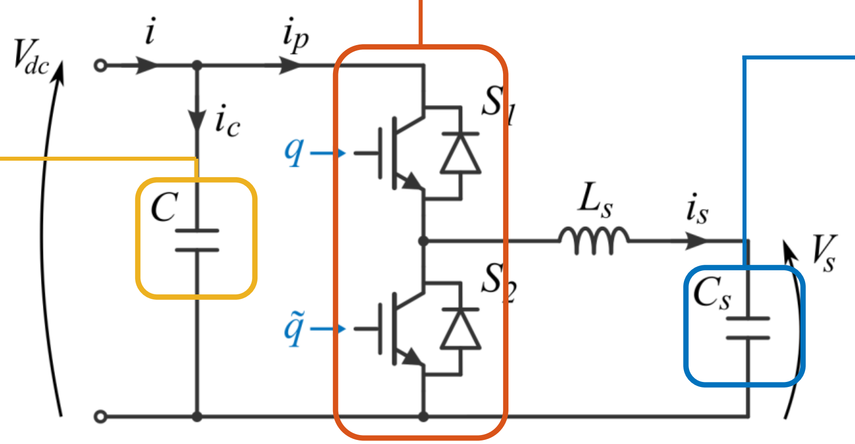
$$\frac{1}{C} = \frac{dV}{dQ} = 0 \quad \rightarrow \quad C = \infty$$

It is possible to try to emulate this behavior by means of an auxiliary circuit connected to the DC bus

Bidirectional DC/DC converter

Bus capacitor

Small, to filter switching ripple



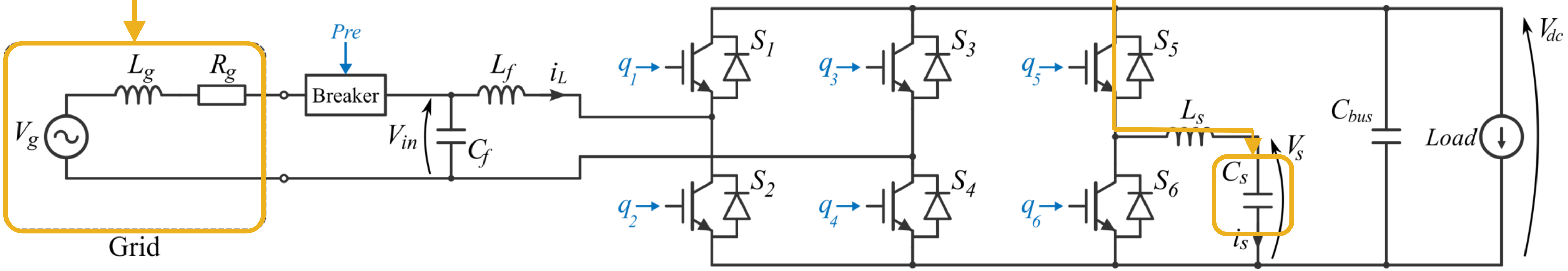
Buffer capacitor

To store ripple energy

$$E_{C_s} = C_s \, V_s \, \Delta V_s$$

Virtual Capacitor

The pulsed energy is stored in the buffer capacitor

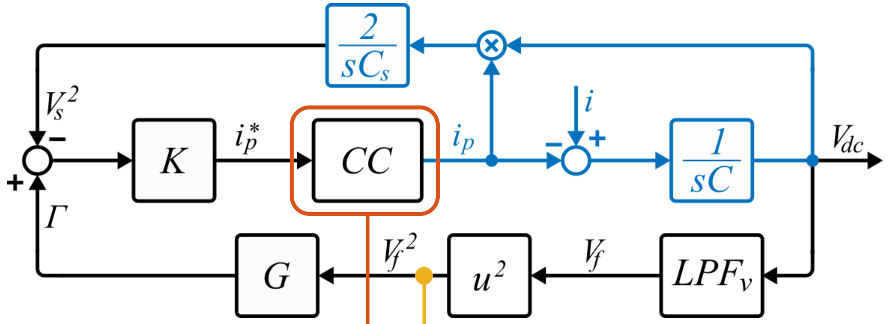


Allow better exploitation of the system capacitance by means of an auxiliary DC/DC converter → Less capacitance needed → Possibility of using film capacitors

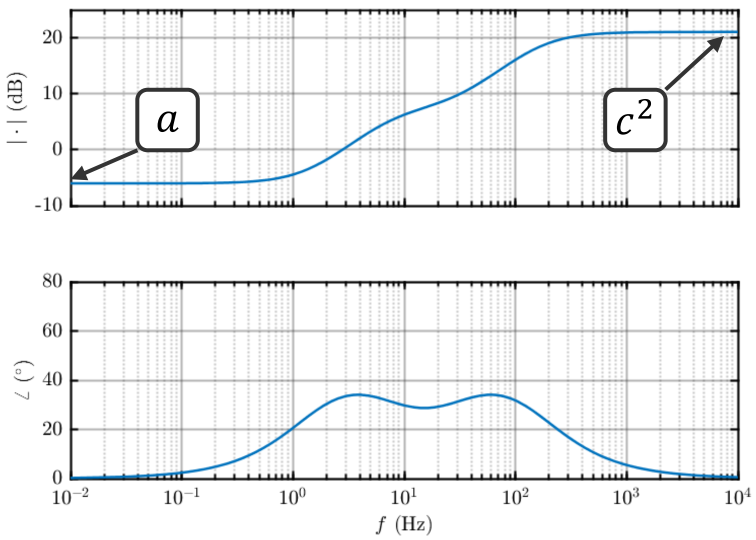
Less capacitance needed → Higher power density

Possibility of using film capacitors → Better reliability

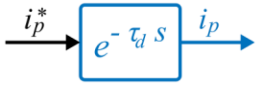
Control Strategy



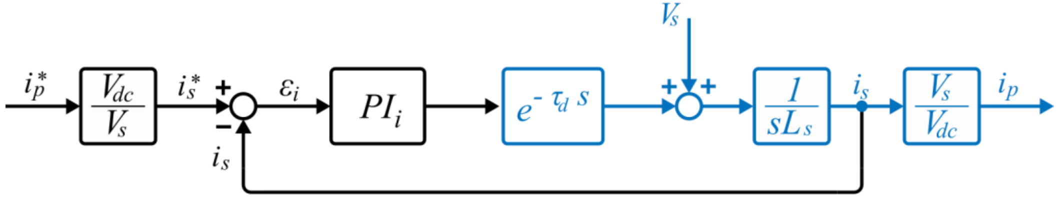
$$G(s) = a\,\frac{c^3\tau s + 1}{c^2\tau s + 1}\,\frac{c\tau s + 1}{\tau s + 1}$$



Current Control

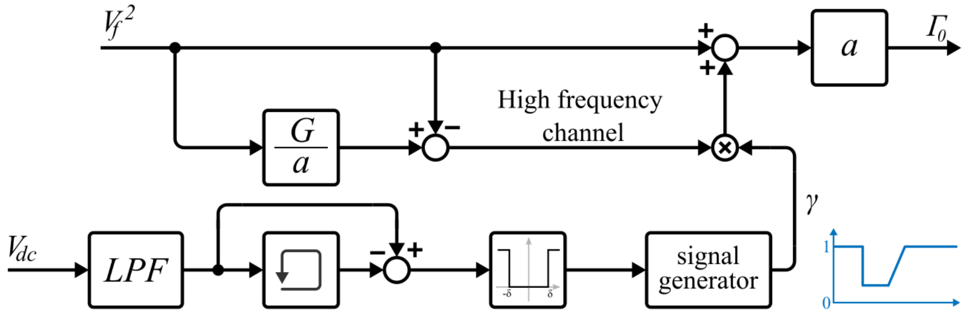


DCM

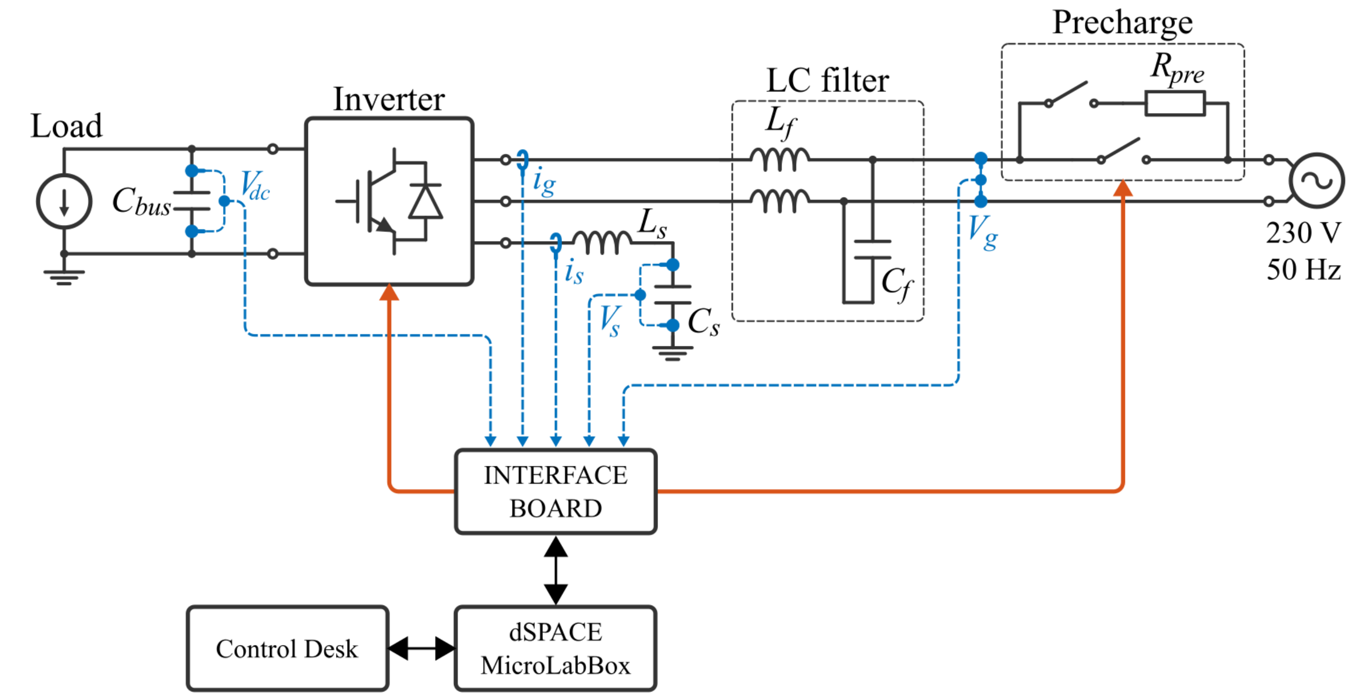


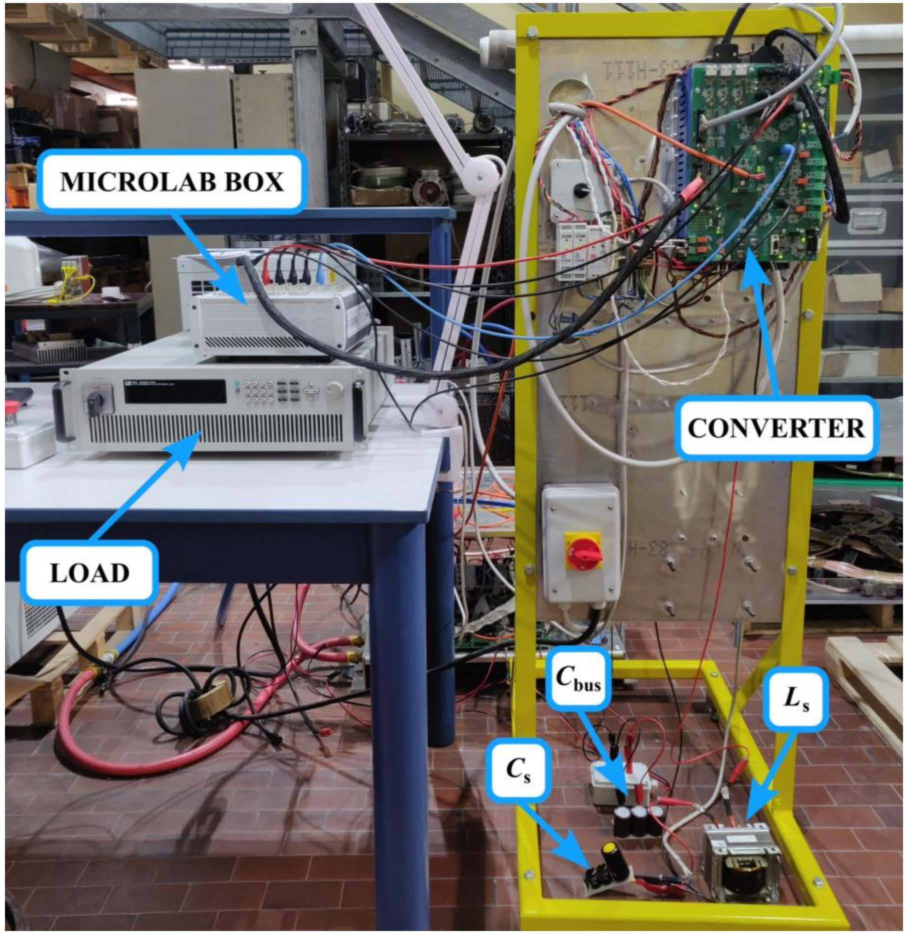
CCM

Load Variation Protection



Laboratory Test Setup





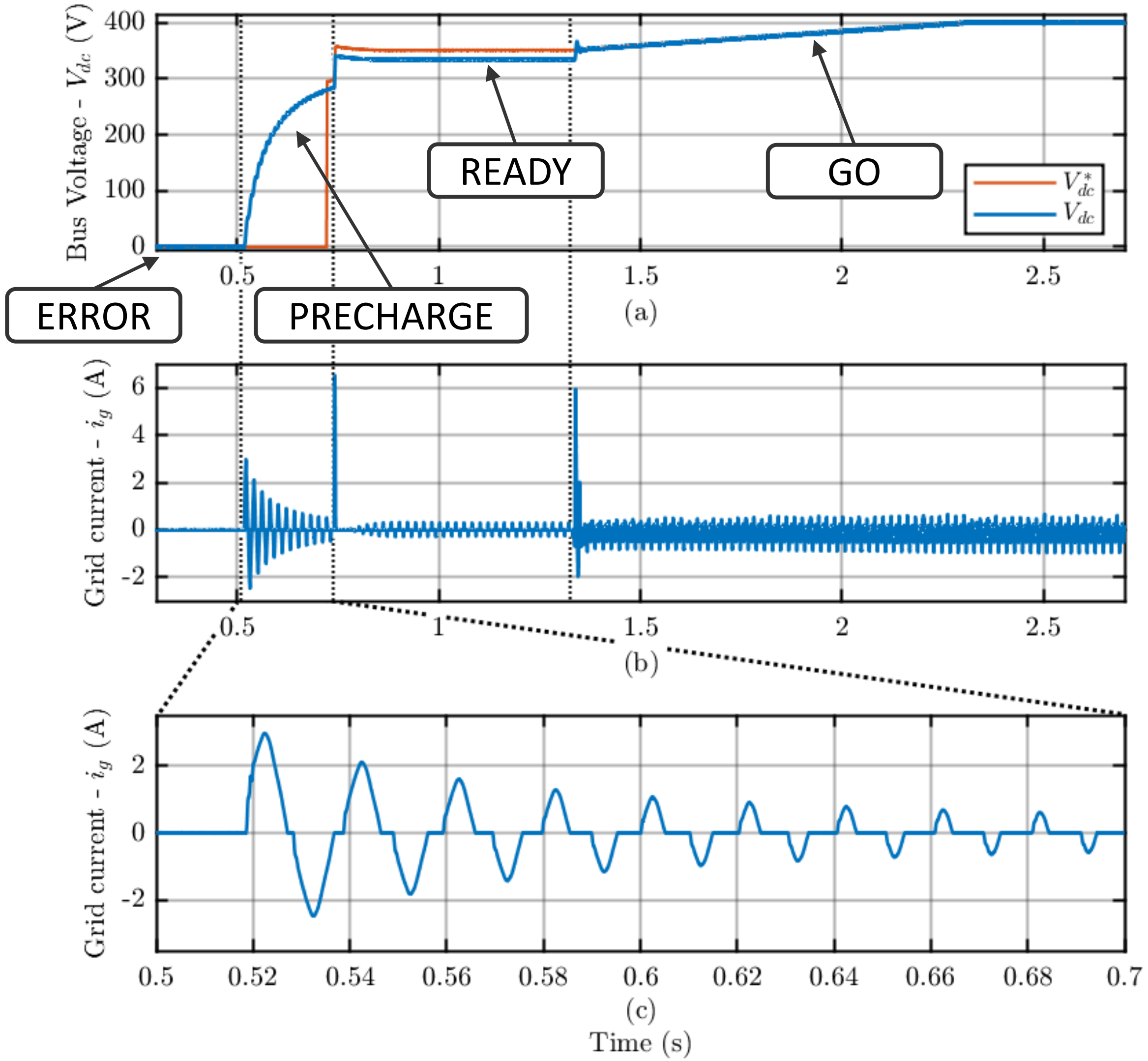
$$f_{sw} = 20\ kHz$$

$$R_{pre} = 15\ \Omega \qquad C_{bus} = 210\ \mu F$$

$$L_f = 2\ mH \qquad C_s = 220\ \mu F$$

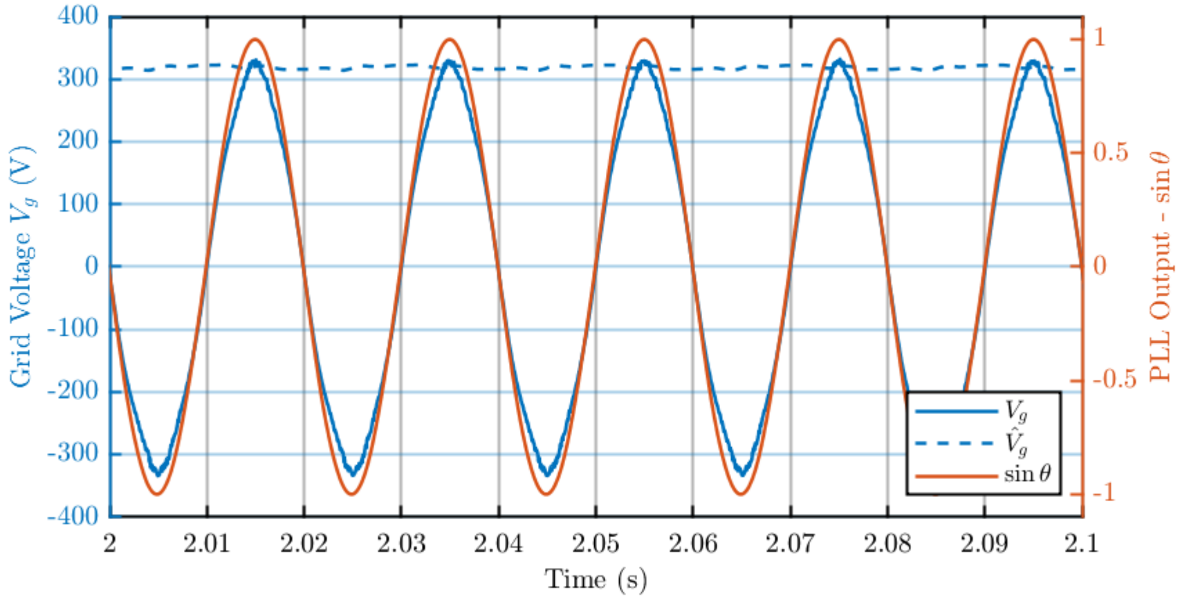
$$C_f = 5\ \mu F \qquad L_s = 6\ mH$$

Experimental Validation



PFC Startup Process

PLL Performance



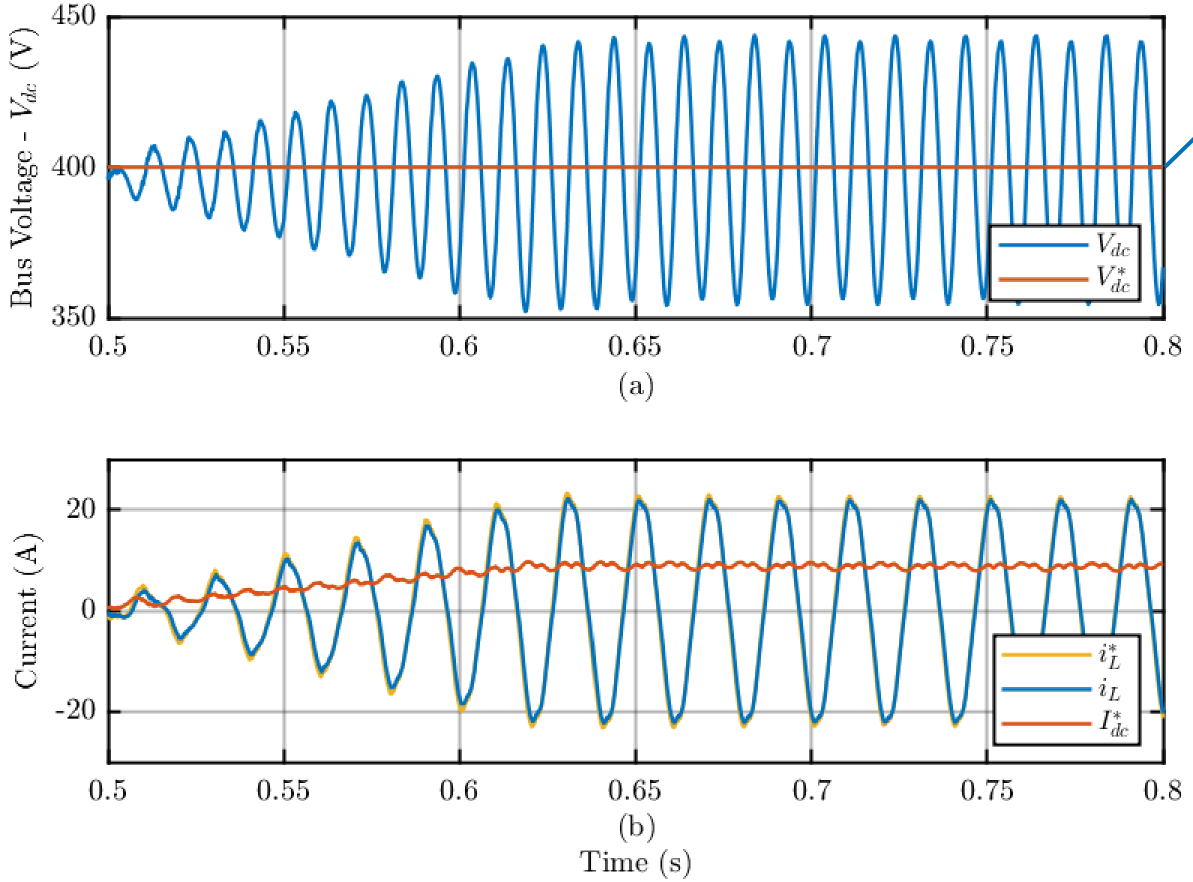
Load Pulse (VC OFF):

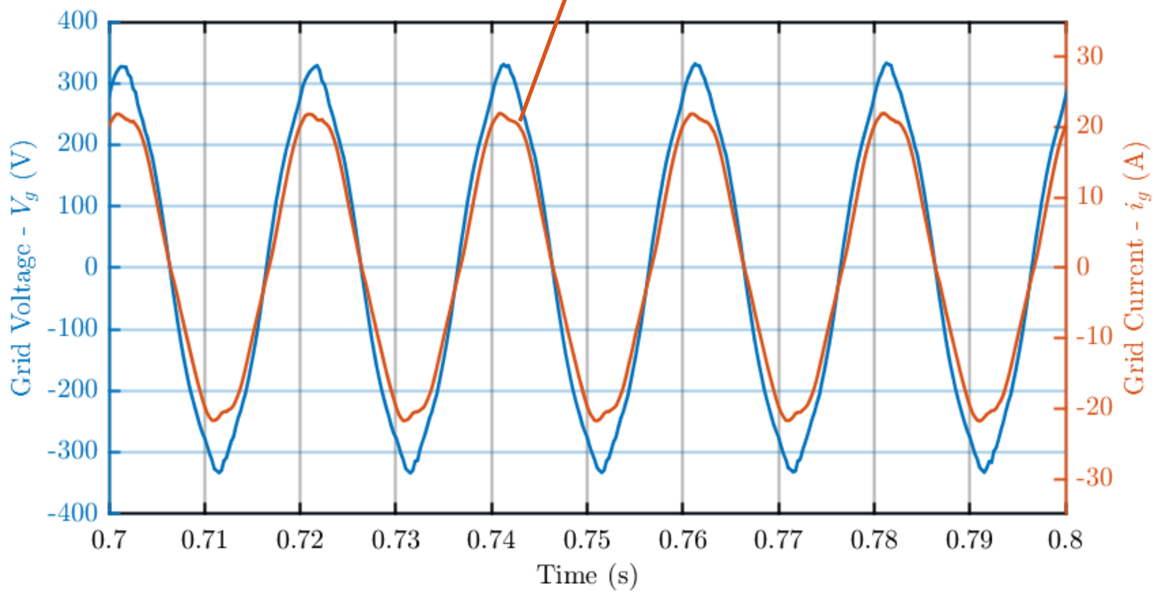
Amplitude: $8.25\ A\ \ (3.3\ kW\ @400\ V)$

Rising and falling rate: $50\ A/s$

DC bus mean voltage equals to the reference
Large ripple because of lack of capacitance

Low distortion current in phase with the voltage absorbed from the grid – THD = 3.2%





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Load Pulse (VC ON):

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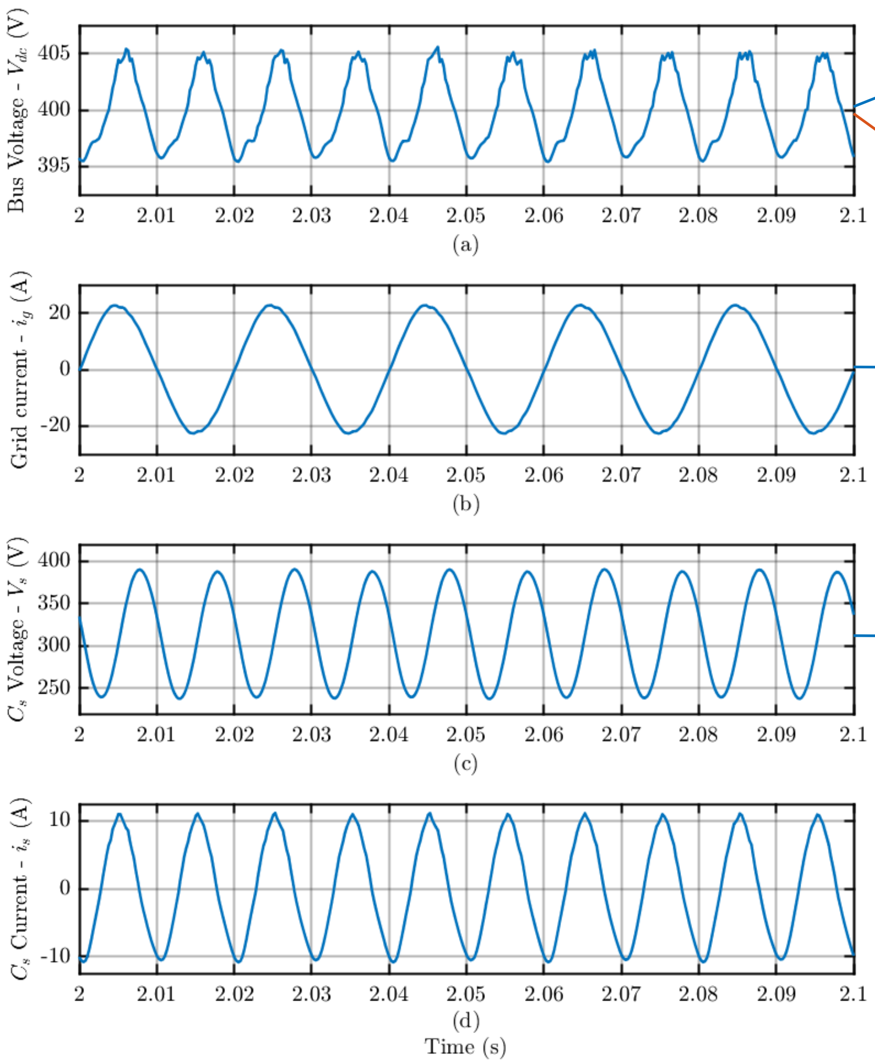


Lower ripple on the DC bus at steady state

Distortion due to dead time and high frequency resonance

Cleaner current absorbed from the grid – THD 2.5%

Large voltage oscillation on the buffer capacitor

Load Variation Protection:

Trigger signal passes threshold value

↓

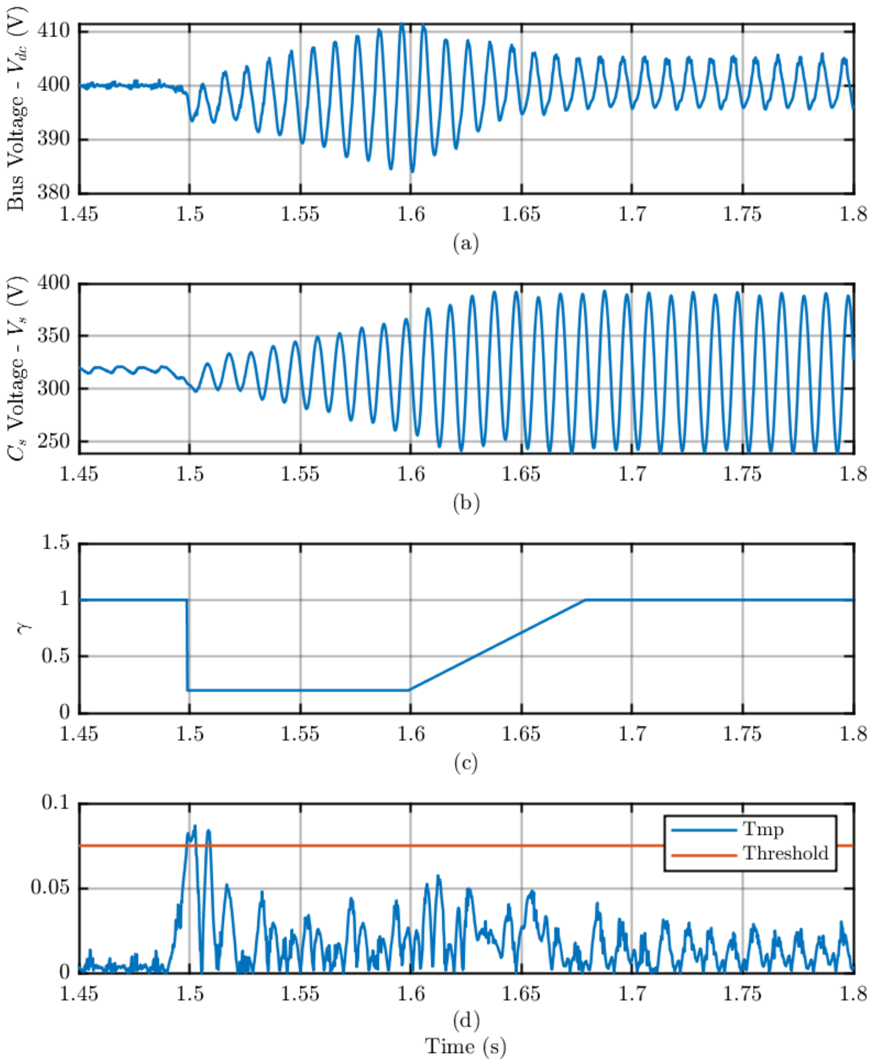
High frequency gain temporary decrease

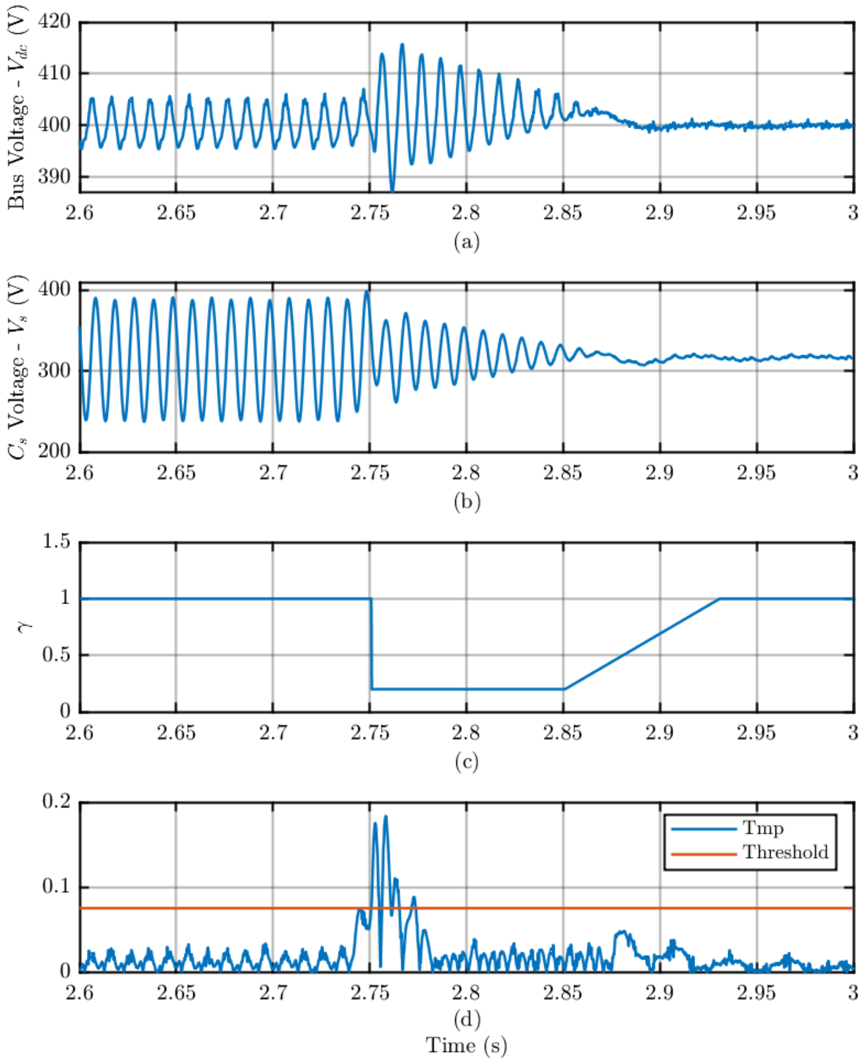
↓

Higher oscillation on the DC-bus and smaller on the buffer capacitor

↓

V_s does not leave the working range



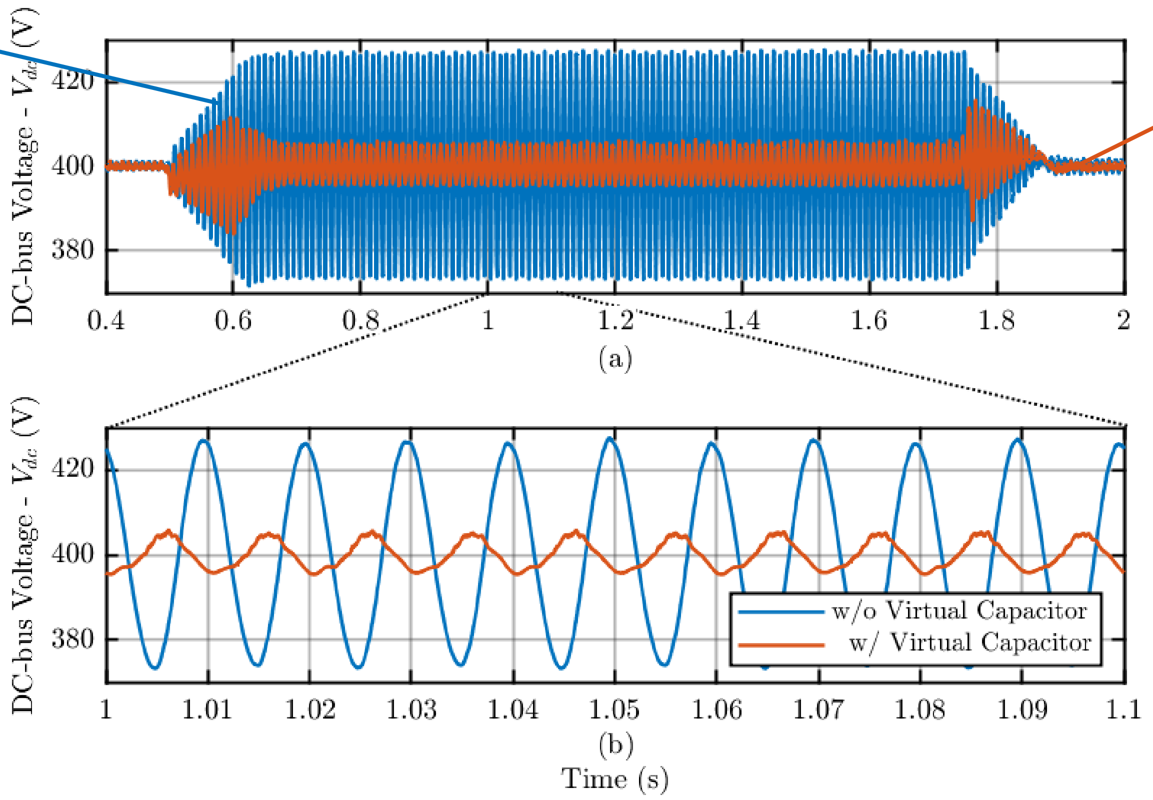


DC Link – VC Comparison

DC Link Approach

$\Delta V = 48\ V$

$C_{bus} = 430\ \mu F$



VC Approach

$\Delta V = 9\ V$

$C_{bus} = 220\ \mu F$

$C_s = 210\ \mu F$

80% reduction of the ripple at steady state with the same total capacitance

Conclusions

Conclusions:

- AFE + VC good candidate for grid friendly AC/DC converters
- Excellent ripple attenuation with possibility of a Plug n Play application
- VC can reduce the need of capacitors on the DC side → Higher power density

Future developments:

- Realization of a VC prototype with SiC MOSFET technology to improve the control performances with higher switching frequency

Personal contribution:

- Bibliographic analysis concerning active rectification and impedance emulation
- Sizing of the main components of the system
- Definition and implementation of the control logic of the two devices (PFC and VC)
- Modelling and simulation, both electrical and thermal, of the system on PLECS environment
- Experimental validation

Thanks for the attention!