Virtual Capacitors for Single Phase Power Electronics Converters

Candidate: Luca Landrino **Supervisor:** Prof. Radu Bojoi **Co-Supervisor:** Dr. Fabio Mandrile

***Abstract*—It is known that there exist second-order harmonic current and corresponding ripple voltage on DC bus for single phase AC/DC active rectifiers. This low frequency ripple is normally filtered using electrolytic capacitors which results in low power density and low reliability. This thesis presents the design of an active rectifier with boost Power Factor Correction (PFC) stage and an active ripple energy storage method that can effectively reduce the needed capacitance, namely Virtual Capacitor (VC). Design consideration and control method are provided and validated through simulation and a 3.3 kW experimental prototype.**

I. Introduction

Nowadays more and more electronic loads are connected to single phase grids, from power supplies for personal computers or laptops to larger appliances with motors controlled by inverters or battery charger for electric vehicles. All these electric appliances requires a conversion stage to transform the alternating current supplied by the network to a direct current. To perform this AC/DC conversion, while ensuring a grid current with low distortion (THD), it is possible to use active rectifier. The output of these converters is then filtered by large DC capacitors, sized to filter the pulsating power at double the grid frequency, typical of single phase systems. However, these capacitors are known to have a relatively low reliability and to be bulky, resulting in poor power density. To overcome this problem, it is possible to exploit a bidirectional converter and an auxiliary circuit in the configuration of a Virtual Capacitor, whose design is the goal of this thesis.

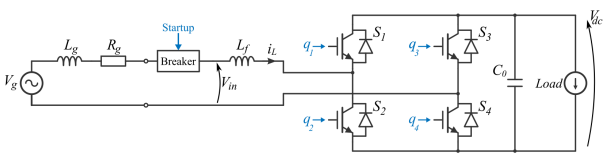

Figure 1: PFC converter connected to the grid.

II. PFC Converter and Grid Synchronization

For the purpose of the thesis, the chosen topology for the PFC is an H-bridge. The control philosophy consists in a cascaded structure with an inner grid current loop regulated by a P-Res controller, whose reference is generated by the outer voltage loop PI regulator together with the Phase Locked Loop (PLL) output that provides synchronization with the grid voltage.

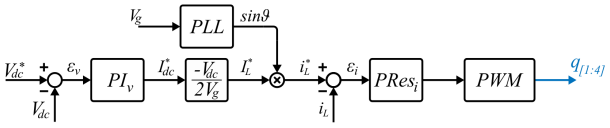

Figure 2: Block diagram of the PFC Control philosophy

III. Virtual Capacitor

The virtual capacitor circuit consists of a bidirectional converter connected to the DC bus, with the output connected to an auxiliary inductor and a buffer capacitor in which to store ripple energy from the DC bus, as shown in Fig.3.

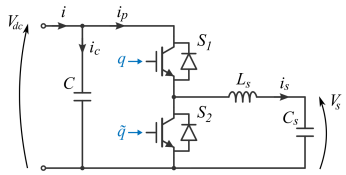

Figure 3: Virtual capacitor auxiliary circuit.

Different types of controls have been investigated for this device. The one which provided the best performance is shown in Fig.4, where the CC block represents the current control that can be open loop in case of a Discontinuous Conduction Mode (DCM), o closed loop based on a PI regulator for Continuous Conduction Mode (CCM). Both cases has been investigated in the thesis.

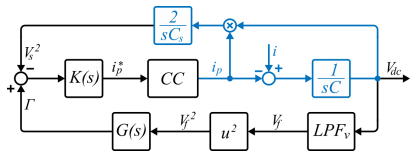

Figure 4: Overall block diagram of the virtual capacitor: black is control, blue is the plant.

Knowing that the voltages V_s and V_{dc} oscillates at the same frequency but with different magnitudes and DC offsets, the reference Γ for V_s^2 can be derived from V_{dc}^2 with a variable gain, lower at low frequencies and much higher in the frequency of interest, represented by a second order Lead Lag $G(s)$. The regulator $K(s)$ can also be implemented with a Lead Lag or with a PI regulator, as long as it can track the reference quickly. Again, both cases has been investigated. In the summary, only the Lead Lag results are presented, as they featured the best performance.

IV. Experimental Results

Referring to the circuits in Fig.1 and Fig.3, the experimental setup shown in Fig.5 was built. A standard three-phase inverter was exploited to implement the converters, using two legs for the PFC and the third one for the virtual capacitor. Due to the IGBT technology of the inverter switch, the switching frequency has been limited to 20 kHz.

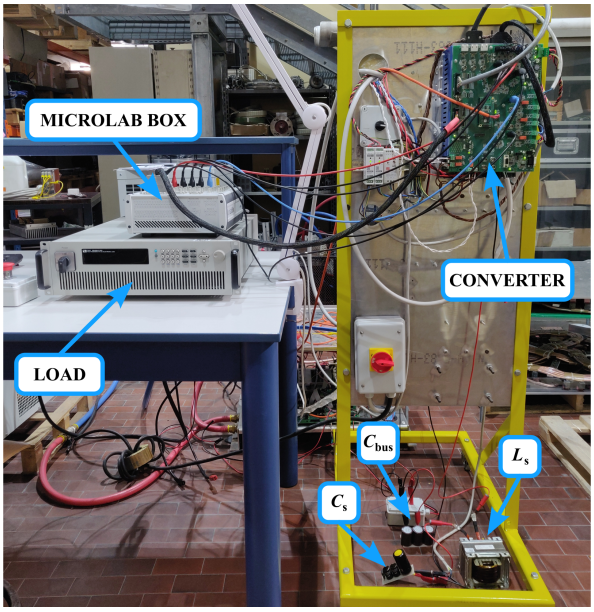

Figure 5: Laboratory setup used for the experimental tests.

The experimental results demonstrate the effectiveness of the VC. The tests under load were performed by applying a 1.25 s pulsed load equal to 3.3 kW (8.25 A) with rising and falling rate of 50 A/s.

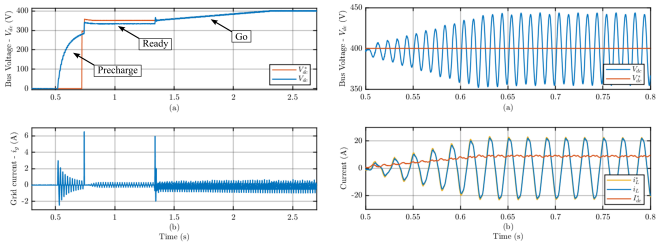

Figure 6: Startup process (left) for the PFC and transient start (right) for a 3.3 kW load.

In Fig.6 is shown the startup process for the PFC and a load transient with no Virtual capacitor. The voltage loop keep the mean voltage at the reference value but because of the low capacitance of the DC-link (210 μF) the voltage oscillation are really large (90 V peak-to-peak).

By activating the virtual capacitor, the ripple on the DC bus is considerably attenuated and the capacitance seen by the circuit is 6.6 times higher than the installed one (equivalent to 2.85 mF instead of 430 μF).

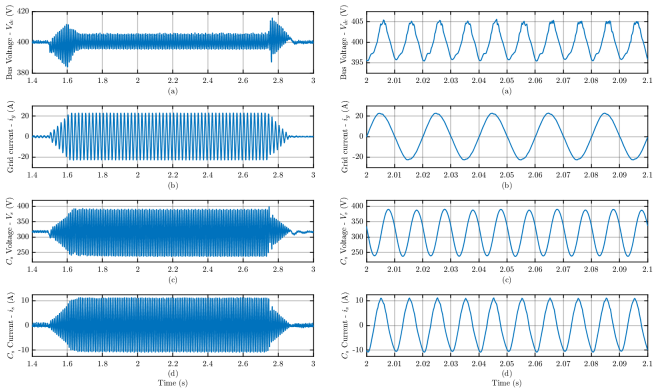

Figure 7: Main quantities measured during a power transient, with a zoomed version at steady state on the right.

The difference in ripple attenuation between a passive vs. an active use of the capacitance is 80% (48 V vs 9 V peak-to-peak) as shown in Fig.8.

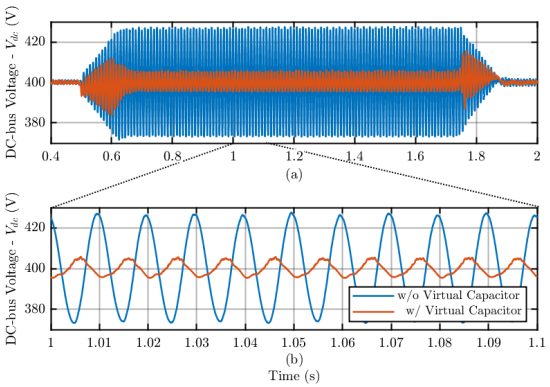

Figure 8: Differences between a passive usage of the system capacitance (blue) and an active one by means of the VC (red).

V. Conclusions

The implementation of the PFC and virtual capacitor models and the simulations carried out with the PLECS software have found confirmation in the experimental practice, validating the design and control both in terms of steady-state and dynamic performance. The device is able to attenuate the second harmonic ripple 80% more than a normal DC link with the same capacitance, reducing the peak value from 24 V to 4.5 V.

My personal contributions for this thesis work are:

- Study of the literature concerning active AC/DC conversion and Active Impedances Emulation.
- Definition of the control logic to be implemented separately on the two devices (PFC and VC) with consequent writing of the code in C language.
- Modelling of the constituent elements of the system and validation of the models and control strategies by means of simulations, both electrical and thermal, in the PLECS environment.
- Experimental validation of the PFC + VC system to determine its correct functioning and allowing a study of the real characteristics.