

High-performance Digital Control of Power Converters

Candidate: Samuele FABBRI **Supervisors:** Prof. Salvatore MUSUMECI, Dr. Fabio MANDRILE

Abstract—In this thesis, the Simulink HDL Coder tool effectiveness is validated for the automatic generation of DC/DC and DC/AC power converters digital control systems VHDL codes. In particular, two different high-performance digital average current control systems are designed and simulated on Simulink. Then, HDL Coder is used to automatically generate the corresponding VHDL code. At last, the control systems are implemented on an FPGA and their correct operation is experimentally tested on the corresponding power converter. First, a PWM modulator and a current controller are implemented for a four-quadrant H-bridge converter. Then, the same system is extended for the current control of a three-phase inverter, designing a carrier-based space vector PWM modulator. In both modulation cases, a multisampling double-update strategy is exploited. Finally the digital current control system is adapted to the torque control of an electric motor, deploying also an external speed loop.

I. INTRODUCTION AND PURPOSE OF THE THESIS

When implementing a power converter digital control system, one of the usual main drawbacks is the required programming time which introduces a delay between the system design and simulation and the experimental phase. An effective way to minimize it is achieved by specific tools which automatically generate the needed code for the target platform, hence, for instance, either C code for a microcontroller or HDL code for an FPGA.

The main goal of this thesis is to validate one of these tools, hence Simulink HDL Coder, which is exploited to produce synthesizable VHDL code: in particular, two different average current control systems are implemented and simulated on Simulink for two pulse width modulated power converters with inductive load, namely an H-bridge converter and a three-phase inverter. After that, the automatically generated VHDL codes are implemented on a Xilinx FPGA and the two control systems are experimentally validated on the corresponding converter implemented on a power stack.

Furthermore, a dSPACE rapid prototyping system is adopted to generate the signals which are needed for the control system operation and to analyze the system main quantities by means of a visual interface. Finally, the designed average current control systems are adapted for the torque control of a permanent magnet assisted synchronous reluctance (PMASR) motor and an external

speed control loop is added. The experimental setup is shown in Figure 1.

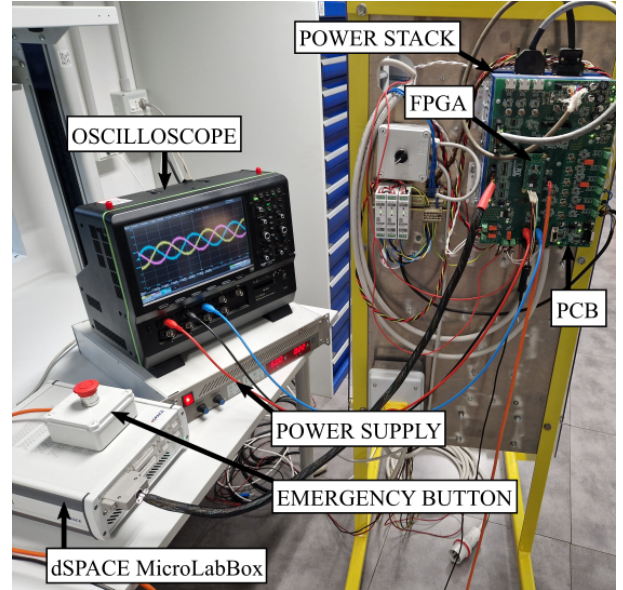


Figure 1: Experimental setup.

II. AVERAGE CURRENT CONTROL SYSTEM

When designing a power converter average current digital controller with a PWM modulator which exploits a triangular carrier, some fundamental aspects to be considered are the current sampling operation and the modulator control voltage update. Among the many possible solutions, the multisampling double-update strategy, whose operation is summarized in Figure 2, is adopted in this work, since it is comparable in terms of modulation delay with other simpler strategies but introduces some advantages, namely the non-requirement of synchronization with the triangular carrier and a fast overcurrent situation detection. Moreover, the multiple-crossing of the carrier is avoided with respect to other multisampling strategies. Basically, considering a case in which a single current is controlled, the current is sampled N_{MS} times inside a switching period by means of an ADC: after that, a moving average filter is exploited to obtain the current average value, which is used for the operation of the closed-loop control system, reported in Figure 3, which imposes it to be equal to a reference value. As highlighted, it is composed of a PWM modulator and a current controller, which is in turn based on a PI regulator with a proper clamping-based anti-windup

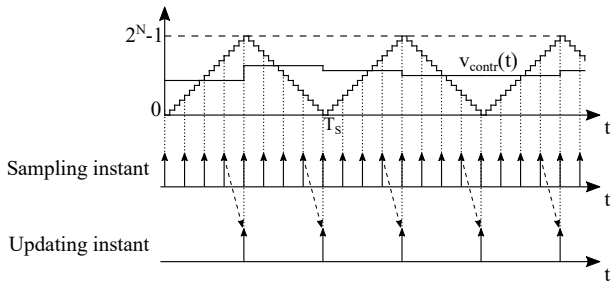


Figure 2: Multisampling double-update mode example.

solution, whose parameters are chosen in order to obtain a 500 Hz bandwidth as a function of the converters inductive load value. The control voltage produced by the current controller is provided to the PWM modulator which compares its value with the triangular carrier in order to generate the switching functions of the transistors inside the converter. The control voltage value is updated in correspondence of every maximum and minimum value of the triangular carrier, hence twice per switching period.

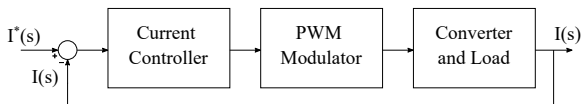


Figure 3: Overall closed-loop system block scheme.

III. H-BRIDGE CONVERTER CONTROL

The first converter to be tested is the H-bridge converter with inductive load, which is implemented by driving the first two switching legs of the three-phase inverter depicted in Figure 5. Various DC reference current values have been tested and the load current was measured by means of a current probe. The experiment results are depicted in Figure 4, where the reference values are reported in the legend. As shown, the current average values track the reference value with good approximation.

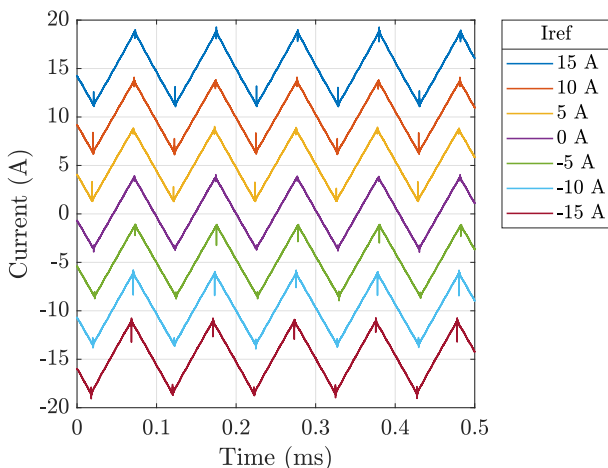


Figure 4: H-bridge converter load current waveforms.

IV. THREE-PHASE INVERTER CONTROL

The second converter which has been tested is a three-phase inverter with a star connected inductive load, as depicted in Figure 5. For the control system implementation, one solution can be that of replicating that depicted in Figure 3 for each phase; anyway, a much better performing system can be obtained by implementing the Clarke's and Park's transforms, since in that case only two PI regulators are needed and each one works in the dq-frame with a DC reference signal instead of a sinusoidal one, providing a null steady-state error. Moreover, a carrier-based space vector PWM modulator is designed.

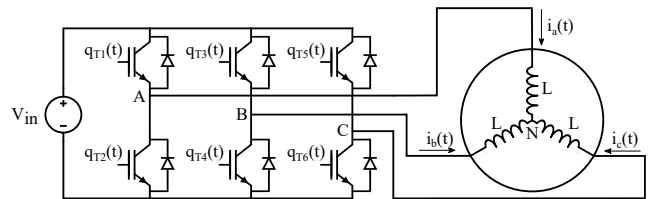


Figure 5: Three-phase inverter topology.

An example of operating waveforms is reported in Figure 6, when a 15 A d-axis and a 0 A q-axis reference currents are provided and a 50 Hz fundamental frequency is requested. Consequently, the expected result is to obtain 50 Hz three-phase currents whose amplitude is 15 A. As can be seen, the wanted behavior is achieved with good approximation.

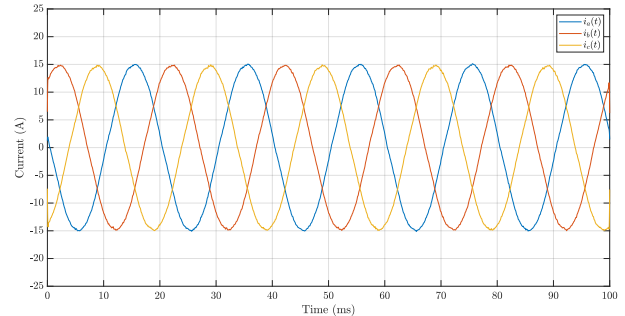


Figure 6: Three-phase inverter current waveforms.

V. TORQUE CONTROL OF AN ELECTRIC MOTOR

As a final practical application, the three-phase inverter average current controller is exploited for the torque control of a permanent magnet assisted synchronous reluctance (PMASR) motor. The whole torque control system block scheme is shown in Figure 7. As shown, a Maximum Torque Per Ampere (MTPA) look-up table is exploited in order to provide the dq-frame reference current values for every requested torque value. Moreover, an encoder is deployed to derive the mechanical rotating angle and, consequently, the electrical angle, which is used for the transforms inside the current controller. For this purpose, the setup depicted in Figure 8, composed of the Motor Under Test (MUT) and a Driving Machine (DM) is exploited.

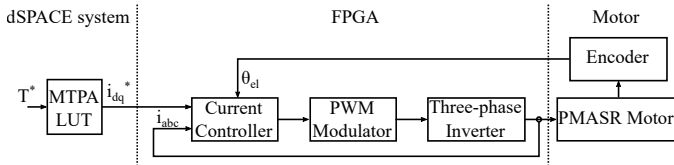


Figure 7: Torque control system block scheme.

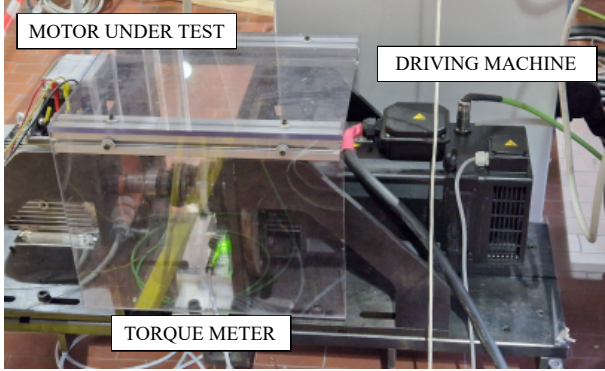


Figure 8: Motor Under Test and Driving Machine setup.

The two motors are linked by means of a shaft on which a torque meter is placed. In a first experiment, the DM imposes a shaft rotation equal to 500 revolutions per minute (rpm) and a 10 Nm torque is requested to the MUT. In Figure 9 the torque meter measurement is reported: since it is affected by oscillations, as it can be seen by looking at the instantaneous waveform, the torque average value in the considered time interval is computed and plotted. As reported, the wanted average torque is generated.

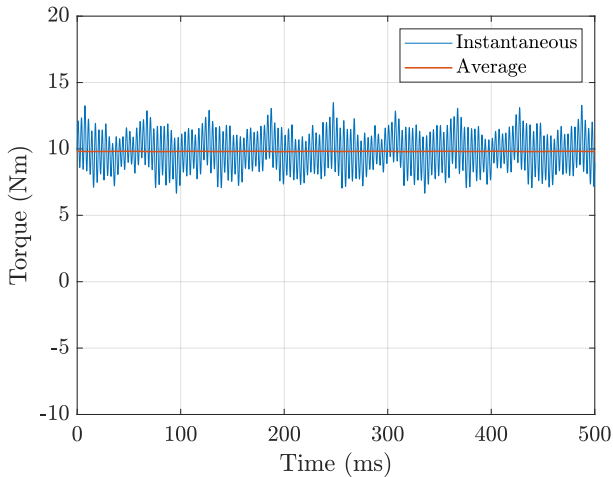


Figure 9: Torque regulation example.

In a second test, an external speed control loop, based on a PI regulator, was inserted in the control system: in this case, the motor speed is compared with a reference value and the corresponding reference torque is produced. Then, the MTPA look-up table is exploited to provide the dq-frame reference current values. The DM is used to impose only a certain load torque and the MUT regulates

its generated torque in order to obtain the reference speed. Starting from a still shaft, the speed is imposed to be 500 rpm and then 0 rpm. The result of the experiment is depicted in Figure 10, which shows that the correct operation is obtained.

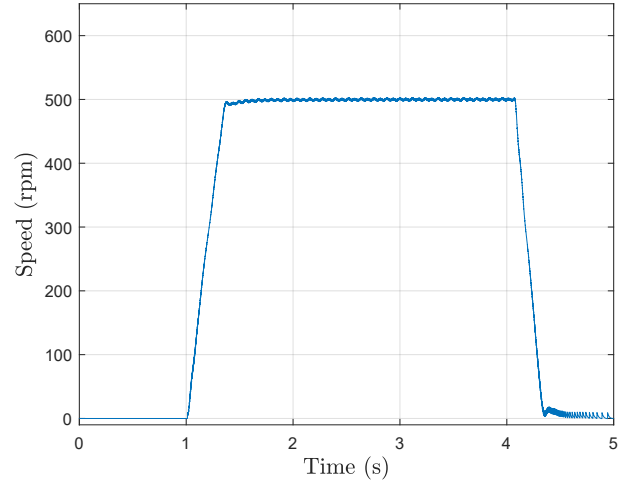


Figure 10: Speed regulation plot.

VI. CONCLUSIONS

In this thesis work, the Simulink HDL Coder automatic code generation tool has been used in order to minimize the programming time which is necessary from the simulation of a power converter control system to the experimental phase. Every designed control system was implemented in Simulink and the corresponding VHDL code was automatically generated. However, in order to obtain the control systems wanted behavior, a few changes in the produced codes needed to be introduced. Anyway, by exploiting this tool the delay between simulation and experimental validation is minimized. The H-bridge converter and the three-phase inverter current control systems and the PMASR motor torque control system, equipped also with an external speed control loop, have been experimentally tested. In particular, in this thesis work, I:

- designed the presented power converters control systems;
- simulated each component of the control systems;
- generated the VHDL code corresponding to each control system through Simulink HDL Coder and modified it to obtain the wanted operation;
- implemented each control system on the FPGA;
- wrote the VHDL codes for additional blocks which were inserted in the system for instance for protection reasons or to manage the acquisitions;
- experimentally validated every designed control system.

Since as previously shown every control system correct behavior has always been obtained, the Simulink HDL Coder tool effectiveness is validated.