Multilevel PFC Control Unit

Candidate: Alessio SABETTA **Supervisor:** prof. Fabio MANDRILE **Co-supervisor:** prof. Fausto STELLA

***Abstract*—This thesis addresses the design of a control unit for a high-frequency GaN-based multilevel flying-capacitor Power Factor Correction (PFC) converter. The work covers two complementary aspects: the hardware redesign of the control board and the development of the control algorithm. Two separate boards have been developed: one required for basic operation, and an optional board providing galvanic isolation. A cascaded control architecture has been implemented and validated through PLECS simulations.**

I. INTRODUCTION

Energy efficiency and power quality have become critical requirements in modern power systems. PFC converters are essential to ensure that the current drawn from the AC grid is in phase with the grid voltage and has low harmonic content.
This thesis starts from an existing platform (EPC91107KIT, shown in Fig. 1) and it has the goal of **redesigning the hardware of its control unit and to develop a control algorithm for the converter.** The electrical specifications of the PFC converter include an input supply voltage of 230 $V_{AC,RMS}$, an output voltage of 400 V_{DC}, a power of 5 kW, and a switching frequency of 140 kHz.
To achieve this goal, I first developed the PCB layout of the two boards of the control unit to make them compatible with the power hardware. Then, I implemented in PLECS the PFC cascaded control to validate it and verify its execution time.

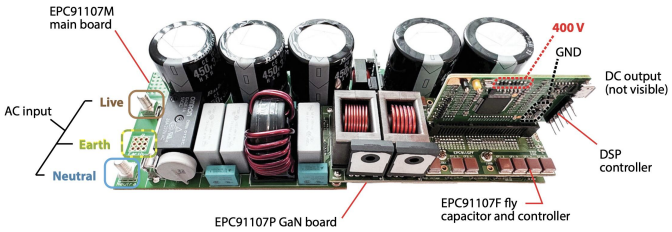


Figure 1: Structure of the EPC PFC converter.

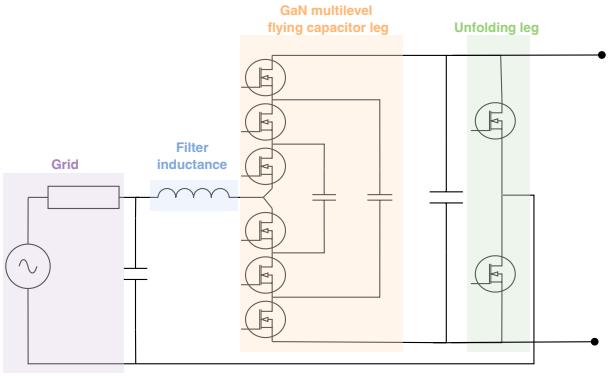


Figure 2: Electrical schematic of the EPC PFC converter.

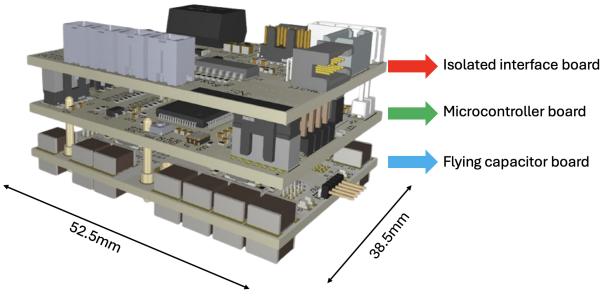
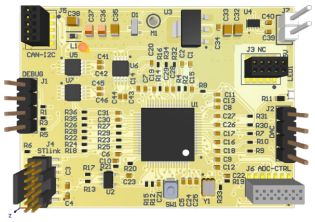
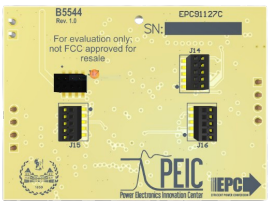


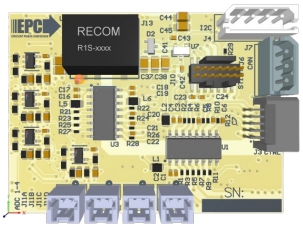
Figure 3: 3D rendering of the multi-board assembly



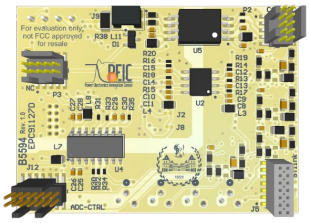
(a) MCU Board — top view



(b) MCU Board — bottom view



(c) Isolated Board — top view



(d) Isolated Board — bottom view

Figure 4: 3D rendering of the two custom PCBs.

II. SYSTEM ARCHITECTURE

This PFC features a multilevel flying capacitor topology with unfolding, as shown in Fig. 2. The power hardware was not changed during this thesis, since the focus was on the control board. This control unit, which was previously positioned vertically above the flying capacitor board, has been divided into two separate boards, positioned as shown in Fig. 3. This approach has the advantage of optimizing the overall volume.
The first board (Fig. 4a and 4b) provides the basic control functions to run the converter. Therefore, it hosts the STM32G4 microcontroller, the signal buffers for feedback signals, the power supply, and the connectors to the power stage. The second board (Fig. 4c and 4d) is dedicated to the optional isolated interface to external devices. It integrates an isolated DC/DC converter supplying signal isolators, additional ADCs, and user connectors. This configuration enables the programmer to be connected to the microcontroller even while the converter is operating, effectively separating the high-voltage power stage from the low-voltage control domain. For both boards, a six-

layer stack-up was chosen to ensure adequate signal integrity and easiness of routing.

III. Control Architecture

The control algorithm, shown in Fig. 5, is made out of several functional blocks. First, the converter is controlled with cascaded DC voltage and AC current loops. The current loop tracks a sinusoidal reference in phase with the grid voltage, which is extracted by a PLL. Additional functions are related to the correct startup and protection of the converter. In particular, I implemented a state machine to manage the DC capacitors precharge and initial synchronization of the PFC. The target control execution frequency is 1/5 of the switching frequency (i.e., 28 kHz).

Regarding the AC current control, two different techniques were explored:

1) **PI-Resonant regulator:** A conventional linear controller tuned at fundamental grid frequency, enhanced with multiple resonant cells for higher order harmonics;
2) **Deadbeat control:** A model-based predictive regulator is used to improve the dynamic of the conventional PI-Resonant controller. This has an advantage on the controller dynamics in case of rapid grid voltage variations, such as voltage dips.

IV. Results

I validated the control in PLECS simulations considering two scenarios:

1) Normal operation with non-distorted grid with short circuit ratio (SCR) 100 and X/R ratio equal to 0.1;
2) Operation in case of grid voltage dip (0.8 pu residual voltage).

Figure 6 shows the grid current and voltage in the first scenario when running at full power of 5 kW. It can be observed that the grid current is perfectly in phase with the voltage, with a measured current THD of 0.3% when using the PI-resonant controller. A higher THD value is obtained with the deadbeat controller (i.e., 4.11%). The reason for this is the not good enough discretization. If a finer discretization step is chosen (i.e., 140 kHz), the waveform quality improves significantly and the THD drops to 1.8%.

The second scenario was tested to highlight the main difference between the two controller implementations. Fig. 7a shows the inadequate response obtained using the resonant controller, whereas Fig. 7b shows the result obtained with the deadbeat control. The conventional control is not able to respond fast enough to the voltage dip, leading to the collapse of the DC voltage. On the other hand, the deadbeat regulator enhances the converter response and limits the decrease in the DC output voltage. The necessity of such high performance controller is due to the very limited filter inductance value of the converter (<14 μH), which poses a significant challenge in terms of needed control dynamics.

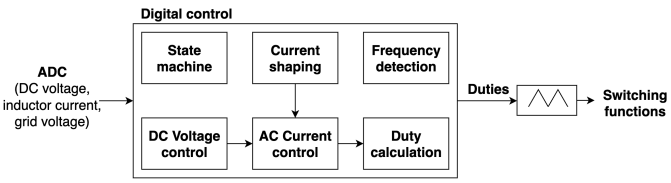


Figure 5: Block diagram of the control algorithm.

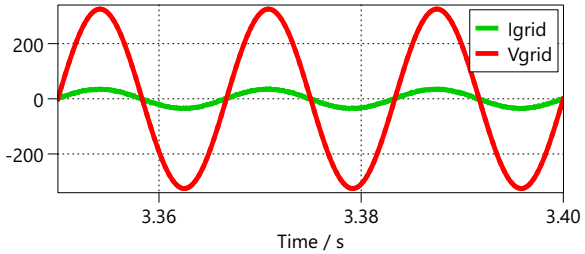
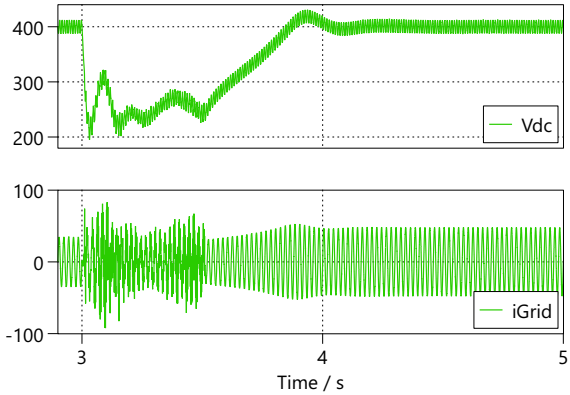
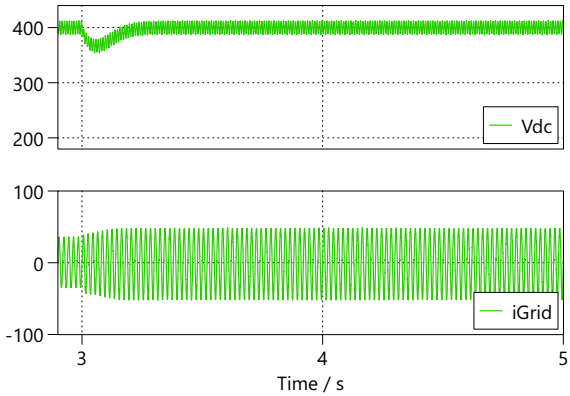


Figure 6: Steady-state waveforms at nominal load with PI-Resonant.



(a) PI Resonant



(b) PI Resonant + Deadbeat

Figure 7: Response to grid voltage dip.

To conclude the validation, the developed control was translated by PLECS into the target MCU to evaluate the required execution time. The measured computation time is 36 μs. This is a blocking factor, since it does not allow the target control frequency of 28 kHz. A possible improvement can be the hand coding of the algorithm to optimize its computation.

V. Conclusions

This thesis presented the redesign of a control unit for a multilevel flying-capacitor PFC converter. Two custom PCBs have been designed for the control implementation. A cascaded control was developed and validated in PLECS, achieving a current THD of 0.3% using PI-resonant regulator, and a current THD of 4.11% using the deadbeat controller.

Although the use of a resonant controller results in a lower THD, this control strategy is not able to effectively manage a voltage dip, whereas deadbeat control excels in this situation.